IN THE SPECIFICATION:

Please amend paragraph [0026] as follows:

FIGs. 2(a)-2~~(d)~~(c) depict various embodiments of the resistor element of the present invention (through cross sectional views) that comprises a multitude of dielectric and conductive layers deposited in a planar configuration;

Please amend paragraph [0037] as follows:

A methodology 200 for forming the resistive structures depicted in Figures 2(a)-2~~(d)~~(c) include a first step 202 of depositing a first interlevel dielectric layer, and, a further step 205 of implementing an atomic layer deposition technique known in the art depositing a resistor film. Next at step 210, using convention photolithographic techniques, the resistor layer is then etched and stripped at designed locations to accommodate the formed via structures. Then, as depicted at step 220, a further interlevel dielectric level may be deposited with alternating resistor films within the trough structure. These steps may be repeated to form the alternating conductive and insulating structures with the formed via structures. Then, as depicted at step 230, a chemical mechanical polish (CMP) technique is used to planarize and clean the structure. As shown in further step 235, a top metal wire structure is deposited and etched with via fill. Known single or dual damascene techniques may be employed.